ABSTRACT

Voltage regulator with an output transistor MP1, including a first PMOS FET, whereby the input voltage Vdd of the voltage regulator is applied to the source of the output transistor MP1 and where the drain of the output transistor MP1 constitutes the output of the voltage regulator. The voltage regulator, furthermore, includes a regulation circuit 1 that may, for example, consist of an error amplifier and that controls the output transistor in such a way that the least possible deviations between the output voltage Vout and the target output voltage are allowed to occur. The voltage regulator includes a switch-on protection circuit that includes a second PMOS FET MP2, whereby the source of the second PMOS FET MP2 is connected to the input voltage Vdd of the voltage regulator, the drain of the second PMOS FET MP2, by way of a pulldown resistor R3, to a reference potential Vss, and the gate of the second PMOS FET MP2 to the reference potential Vss, and which furthermore includes a third PMOS FET MP3, where the source of the third PMOS FET MP3 is connected to the input voltage Vdd of the voltage regulator, the drain of the third PMOS FET MP3 is connected to the gate of the output transistor MP1, and the gate of the third PMOS FET MP3 is connected to the drain of the second PMOS FET MP2.